CLAIMS

1. An image display apparatus comprising:

a pixel having a drive transistor and a pixel display element which are connected in series between a first power line and a second power line, a holding capacitor connected to a gate electrode of said drive transistor, and a selection transistor connected between a signal line and the gate electrode of said drive transistor; and

control means for turning on said selection transistor thereby to write gradation pixel data in said holding capacitor from said signal line, discharging charges of the gradation pixel data written in said holding capacitor through said drive transistor for a predetermined time, and thereafter floating the gate electrode of said drive transistor thereby to hold the charges of the gradation pixel data stored in said holding capacitor.

2. The image display apparatus according to claim 1, further comprising:

a display panel having a plurality of signal lines to which corresponding gradation pixel data are applied and a plurality of scanning lines to which scanning signals are applied, said pixel being positioned at each of points of intersection between said signal lines and said scanning lines;

a signal line driver for applying said gradation pixel data to said signal lines based on a pixel input signal; and

a scanning line driver for applying said scanning signals to said scanning lines;

wherein said selection transistor has a first drain electrode, a first source electrode, and a first gate electrode, said drive transistor has a second drain electrode, a second source electrode, and a second gate electrode, said holding capacitor holds a voltage between said second gate electrode and said second source electrode, and said pixel display element has a first electrode and a second electrode;

wherein said first drain electrode/said first source electrode is connected to said signal line, said first source electrode/said first drain electrode is connected to said second gate electrode, said first gate electrode is connected to said scanning line, and said selection transistor performs on/off control of a conduction state between said signal line and said second gate electrode based on said scanning signal;

wherein said first power line is connected to said second drain electrode, said second source electrode is connected to said first electrode, and said drive transistor passes an output current controlled based on a voltage held by said holding capacitor from said second source electrode to said first electrode; and

wherein said second power line is connected to said second electrode, and said pixel display element displays a pixel at a gradation based on said output current of said drive transistor.

3. The image display apparatus according to claim 2, wherein said scanning signals are applied to said scanning lines in a preset sequence.

4. The image display apparatus according to claim 2, further comprising:

a plurality of resetting signal lines to which resetting signals are applied; and

a resetting signal line driver for applying said resetting signals to said resetting signal lines;

wherein said pixel has a resetting transistor having a third drain electrode, a third source electrode, and a third gate electrode, and a parasitic capacitor is formed between said first electrode and said second electrode;

wherein said third drain electrode/said third source electrode is connected to said second source electrode, said third source electrode/said third drain electrode is connected to said second power line, said third gate electrode is connected to said resetting signal line, and said resetting transistor performs on/off control of a conduction state between said second source electrode and said second power line based on said resetting signal; and

wherein said control means turns on said resetting transistor thereby to discharge said holding capacitor and said parasitic capacitor, and thereafter turns on said selection transistor.

5. The image display apparatus according to claim 2, further comprising:

a plurality of resetting signal lines to which resetting signals are applied; and

a resetting signal line driver for applying said resetting signals to said resetting signal lines;

wherein said pixel has a resetting transistor having a third drain electrode, a third source electrode, and a third gate electrode, and a parasitic

capacitor is formed between said first electrode and said second electrode;

wherein said third drain electrode/said third source electrode is connected to said second source electrode, said third source electrode/said third drain electrode is connected to said first power line, said third gate electrode is connected to said reset signal line, and said resetting transistor performs on/off control of a conduction state between said second source electrode and said first power line based on said resetting signal; and

wherein said control means turns on said resetting transistor thereby to discharge said holding capacitor and said parasitic capacitor, and thereafter turns on said selection transistor.

6. The image display apparatus according to claim 2, wherein said pixel display element has a parasitic capacitor between said first electrode and said second electrode; and

wherein said control means turns on said resetting transistor and supplies a resetting signal voltage from said signal line thereby to discharge said holding capacitor and said parasitic capacitor, and thereafter writes said gradation pixel data from said signal line in said holding capacitor.

7. The image display apparatus according to claim 2, further comprising a power supply circuit for supplying a first power voltage and a second power voltage respectively for said first power line and said second power line to said display panel;

wherein said pixel display element has a parasitic capacitor between said first electrode and said second electrode; and

wherein said control means sets said first power voltage to a resetting signal voltage thereby to discharge said holding capacitor and said parasitic capacitor, and thereafter turns on said selection transistor thereby to write said gradation pixel data from said signal line in said holding capacitor.

8. The image display apparatus according to claim 1, further comprising:

a display panel having a plurality of signal lines to which corresponding gradation pixel data are applied, a plurality of control lines to which control line drive signals are applied, and a plurality of scanning lines to which scanning signals are applied, said pixel being positioned at each of points of intersection between said signal lines and said scanning lines;

a signal line driver for applying said gradation pixel data to said signal lines based on a pixel input signal;

a scanning line driver for applying said scanning signals to said scanning lines; and

a control line driver for applying said control line drive signals to said control lines;

wherein said pixel has a control transistor having a third drain electrode, a third source electrode, and a third gate electrode;

wherein said selection transistor has a first drain electrode, a first source electrode, and a first gate electrode, said drive transistor has a second drain electrode, a second source electrode, and a second gate electrode, said holding capacitor holds a voltage between said second gate electrode and said second source electrode, and each pixel display element has a first electrode, a

second electrode, and a parasitic capacitor between said first electrode and said second electrode;

wherein said first drain electrode/said first source electrode is connected to said signal line, said first source electrode/said first drain electrode is connected to said second gate electrode, said first gate electrode is connected to said scanning line, and said selection transistor performs on/off control of a conduction state between said signal line and said second gate electrode based on said scanning signal;

wherein said first power line is connected to said second source electrode, said drive transistor passes an output current controlled based on a voltage held by said holding capacitor from said second drain electrode to said first electrode;

wherein said third drain electrode/said third source electrode is connected to said second gate electrode, said third source electrode/said third drain electrode is connected to said second drain electrode, said third gate electrode is connected to said control line, and said control transistor performs on/off control of a conduction state between said second gate electrode and said second drain electrode based on said control line drive signal;

wherein said second power line is connected to said second electrode, and said pixel display element displays a pixel at a gradation based on said output current of said drive transistor; and

wherein said control means turns on said selection transistor and turns off said control transistor thereby to write said gradation pixel data from said signal line in said holding capacitor, turns off said selection transistor and turns on said control transistor thereby to discharge charges of said gradation pixel

data written in said holding capacitor through said drive transistor for a predetermined time, and thereafter turns off said control transistor thereby to float said second gate electrode to hold the charges of said gradation pixel data stored in said holding capacitor.

9. The image display apparatus according to claim 1, further comprising:

a display panel having a plurality of signal lines to which corresponding gradation pixel data are applied, a plurality of control lines to which control line drive signals are applied, and a plurality of scanning lines to which scanning signals are applied, said pixel being positioned at each of points of intersection between said signal lines and said scanning lines;

a signal line driver for applying said gradation pixel data to said signal lines based on a pixel input signal;

a scanning line driver for applying said scanning signals to said scanning lines; and

a control line driver for applying said control line drive signals to said control lines;

wherein said pixel has a control transistor having a third drain electrode, a third source electrode, and a third gate electrode;

wherein said selection transistor has a first drain electrode, a first source electrode, and a first gate electrode, said drive transistor has a second drain electrode, a second source electrode, and a second gate electrode, said holding capacitor holds a voltage between said second gate electrode and said second source electrode, and each pixel display element has a first electrode, a

second electrode, and a parasitic capacitor between said first electrode and said second electrode;

wherein said first drain electrode/said first source electrode is connected to said signal line, said first source electrode/said first drain electrode is connected to said second gate electrode, said first gate electrode is connected to said scanning line, and said selection transistor performs on/off control of a conduction state between said signal line and said second gate electrode based on said scanning signal;

wherein said first power line is connected to said second source electrode, said drive transistor passes an output current controlled based on a voltage held by said holding capacitor from said second drain electrode to said first electrode;

wherein said third drain electrode/said third source electrode is connected to said second gate electrode, said third source electrode/said third drain electrode is connected to said second drain electrode, said third gate electrode is connected to said control line, and said control transistor performs on/off control of a conduction state between said second gate electrode and said first drain electrode based on said control line drive signal;

wherein said second power line is connected to said second electrode, and said pixel display element displays a pixel at a gradation based on said output current of said drive transistor; and

wherein said control means turns on said selection transistor and turns on said control transistor thereby to write said gradation pixel data from said signal line in said holding capacitor, turns off said selection transistor and turns on said control transistor thereby to discharge charges of said gradation pixel

data written in said holding capacitor through said drive transistor for a predetermined time, and thereafter turns off said control transistor thereby to float said second gate electrode to hold the charges of said gradation pixel data stored in said holding capacitor.

10. The image display apparatus according to claim 1, further comprising:

a display panel having a plurality of signal lines to which corresponding gradation pixel data are applied, a plurality of control lines to which control line drive signals are applied, and a plurality of scanning lines to which scanning signals are applied, said pixel being positioned at each of points of intersection between said signal lines and said scanning lines;

a signal line driver for applying said gradation pixel data to said signal lines based on a pixel input signal;

a scanning line driver for applying said scanning signals to said scanning lines; and

a control line driver for applying said control line drive signals to said control lines;

wherein said pixel has a control transistor having a third drain electrode, a third source electrode, and a third gate electrode;

wherein said selection transistor has a first drain electrode, a first source electrode, and a first gate electrode, said drive transistor has a second drain electrode, a second source electrode, and a second gate electrode, said holding capacitor holds a voltage between said second gate electrode and said second source electrode, and each pixel display element has a first electrode, a

second electrode, and a parasitic capacitor between said first electrode and said second electrode;

wherein said first drain electrode/said first source electrode is connected to said signal line, said first source electrode/said first drain electrode is connected to said second drain electrode, said first gate electrode is connected to said scanning line, and said selection transistor performs on/off control of a conduction state between said signal line and said second drain electrode based on said scanning signal;

wherein said first power line is connected to said second source electrode, said drive transistor passes an output current controlled based on a voltage held by said holding capacitor from said second drain electrode to said first electrode;

wherein said third drain electrode/said third source electrode is connected to said second gate electrode, said third source electrode/said third drain electrode is connected to said second drain electrode, said third gate electrode is connected to said control line, and said control transistor performs on/off control of a conduction state between said second gate electrode and said second drain electrode based on said control line drive signal;

wherein said second power line is connected to said second electrode, and said pixel display element displays a pixel at a gradation based on said output current of said drive transistor; and

wherein said control means turns on said selection transistor and turns on said control transistor thereby to write said gradation pixel data from said signal line in said holding capacitor, turns off said selection transistor and turns on said control transistor thereby to discharge charges of said gradation pixel

data written in said holding capacitor through said drive transistor for a predetermined time, and thereafter turns off said control transistor thereby to float said second gate electrode to hold the charges of said gradation pixel data stored in said holding capacitor.

11. The image display apparatus according to claim 1, further comprising:

a display panel having a plurality of signal lines to which corresponding gradation pixel data are applied, a plurality of control lines to which control line drive signals are applied, and a plurality of scanning lines to which scanning signals are applied, said pixel being positioned at each of points of intersection between said signal lines and said scanning lines;

a signal line driver for applying said gradation pixel data to said signal lines based on a pixel input signal;

a scanning line driver for applying said scanning signals to said scanning lines; and

a control line driver for applying said control line drive signals to said control lines;

wherein each pixel has a control transistor having a third drain electrode, a third source electrode, and a third gate electrode, and an input drive transistor having a fourth drain electrode, a fourth source electrode, and a fourth gate electrode;

wherein said selection transistor has a first drain electrode, a first source electrode, and a first gate electrode, said drive transistor has a second drain electrode, a second source electrode, and a second gate electrode, said

holding capacitor holds a voltage between said second gate electrode and said second source electrode, and each pixel display element has a first electrode, a second electrode, and a parasitic capacitor between said first electrode and said second electrode;

wherein said first drain electrode/said first source electrode is connected to said signal line, said first source electrode/said first drain electrode is connected to said third drain electrode/said third source electrode, said first gate electrode is connected to said scanning line, and said selection transistor performs on/off control of a conduction state between said signal line and said third drain electrode/said third source electrode based on said scanning signal;

wherein said first power line is connected to said second source electrode, said drive transistor passes a first output current controlled based on a voltage held by said holding capacitor from said second drain electrode to said first electrode;

wherein said third drain electrode/said third source electrode is connected to said first source electrode/said first drain electrode, said third source electrode/said third drain electrode is connected to said second gate electrode, said third gate electrode is connected to said control line, and said control transistor performs on/off control of a conduction state between said first source electrode/said first drain electrode and said second gate electrode based on said control line drive signal;

wherein said first power line is connected to said fourth source electrode, said fourth drain electrode is connected to said first source electrode/said first drain electrode, said fourth gate electrode is connected to said second gate electrode, said input drive transistor passes a second output current controlled

based on a voltage between said fourth source electrode and said fourth gate electrode from said fourth source electrode to said fourth drain electrode;

wherein said second power line is connected to said second electrode, and said pixel display element displays a pixel at a gradation based on said first output current of said drive transistor; and

wherein said control means turns on said selection transistor and turns on said control transistor thereby to write said gradation pixel data from said signal line in said holding capacitor, turns off said selection transistor and turns on said control transistor thereby to discharge charges of said gradation pixel data written in said holding capacitor through said input drive transistor for a predetermined time, and thereafter turns off said control transistor thereby to float said second gate electrode to hold the charges of said gradation pixel data stored in said holding capacitor.

12. The image display apparatus according to claim 1, further comprising:

a display panel having a plurality of signal lines to which corresponding gradation pixel data are applied, a plurality of control lines to which control line drive signals are applied, and a plurality of scanning lines to which scanning signals are applied, said pixel being positioned at each of points of intersection between said signal lines and said scanning lines;

a signal line driver for applying said gradation pixel data to said signal lines based on a pixel input signal;

a scanning line driver for applying said scanning signals to said scanning lines; and

a control line driver for applying said control line drive signals to said control lines;

wherein said pixel has a control transistor having a third drain electrode, a third source electrode, and a third gate electrode, and an input drive transistor having a fourth drain electrode, a fourth source electrode, and a fourth gate electrode;

wherein said selection transistor has a first drain electrode, a first source electrode, and a first gate electrode, said drive transistor has a second drain electrode, a second source electrode, and a second gate electrode, said holding capacitor holds a voltage between said second gate electrode and said second source electrode, and each pixel display element has a first electrode, a second electrode, and a parasitic capacitor between said first electrode and said second electrode;

wherein said first drain electrode/said first source electrode is connected to said signal line, said first source electrode/said first drain electrode is connected to said third drain electrode/said third source electrode, said first gate electrode is connected to said scanning line, and said selection transistor performs on/off control of a conduction state between said signal line and said third drain electrode/said third source electrode based on said scanning signal;

wherein said first power line is connected to said second source electrode, said drive transistor passes a first output current controlled based on a voltage held by said holding capacitor from said second drain electrode to said first electrode;

wherein said third drain electrode/said third source electrode is connected to said first source electrode/said first drain electrode and said fourth

gate electrode, said third source electrode/said third drain electrode is connected to said second gate electrode, said third gate electrode is connected to said control line, and said control transistor performs on/off control of a conduction state between said first source electrode/said first drain electrode and said second gate electrode based on said control line drive signal;

wherein said first power line is connected to said fourth source electrode, said fourth drain electrode is connected to said first source electrode/said first drain electrode, said fourth gate electrode is connected to said fourth drain electrode, said input drive transistor passes a second output current controlled based on a voltage between said fourth source electrode and said fourth gate electrode from said fourth source electrode to said fourth drain electrode;

wherein said second power line is connected to said second electrode, and said pixel display element displays a pixel at a gradation based on said first output current of said drive transistor; and

wherein said control means turns on said selection transistor and turns on said control transistor thereby to write said gradation pixel data from said signal line in said holding capacitor, turns off said selection transistor and turns on said control transistor thereby to discharge charges of said gradation pixel data written in said holding capacitor through said input drive transistor for a predetermined time, and thereafter turns off said control transistor thereby to float said second gate electrode to hold the charges of said gradation pixel data stored in said holding capacitor.

13. The image display apparatus according to claim 1, wherein said pixel display element comprises an organic electroluminescence element.

14. A control method for an image display apparatus including a pixel having a drive transistor and a pixel display element which are connected in series between a first power line and a second power line, a holding capacitor connected to a gate electrode of said drive transistor, and a selection transistor connected between a signal line and the gate electrode of said drive transistor, comprising:

a pixel data writing step of turning on said selection transistor thereby to write gradation pixel data in said holding capacitor from said signal line;

a discharging step of discharging charges of the gradation pixel data written in said holding capacitor through said drive transistor for a predetermined time; and

after said discharging step, a pixel data holding step of floating the gate electrode of said drive transistor thereby to hold the charges of the gradation pixel data stored in said holding capacitor.

15. The control method according to claim 14, wherein said image display apparatus further includes:

a display panel having a plurality of signal lines to which corresponding gradation pixel data are applied and a plurality of scanning lines to which scanning signals are applied, said pixel being positioned at each of points of intersection between said signal lines and said scanning lines;

a signal line driver for applying said gradation pixel data to said signal lines based on a pixel input signal; and

a scanning line driver for applying said scanning signals to said scanning lines;

wherein said selection transistor has a first drain electrode, a first source electrode, and a first gate electrode, said drive transistor has a second drain electrode, a second source electrode, and a second gate electrode, said holding capacitor holds a voltage between said second gate electrode and said second source electrode, and said pixel display element has a first electrode and a second electrode;

wherein said first drain electrode/said first source electrode is connected to said signal line, said first source electrode/said first drain electrode is connected to said second gate electrode, said first gate electrode is connected to said scanning line, said selection transistor performs on/off control of a conduction state between said signal line and said second gate electrode based on said scanning signal;

wherein said first power line is connected to said second drain electrode, said second source electrode is connected to said first electrode, and said drive transistor passes an output current controlled based on a voltage held by said holding capacitor from said second source electrode to said first electrode; and

wherein said second power line is connected to said second electrode, and said pixel display element displays a pixel at a gradation based on said output current of said drive transistor.

16. The control method according to claim 15, wherein said scanning signals are applied to said scanning lines in a preset sequence.

17. The control method according to claim 15, wherein said image display apparatus further includes:

a plurality of resetting signal lines to which resetting signals are applied; and

a resetting signal line driver for applying said resetting signals to said resetting signal lines;

wherein each pixel has a resetting transistor having a third drain electrode, a third source electrode, and a third gate electrode, and a parasitic capacitor is formed between said first electrode and said second electrode;

wherein said third drain electrode/said third source electrode is connected to said second source electrode, said third source electrode/ said third drain electrode is connected to said second power line, said third gate electrode is connected to said reset signal line, and said resetting transistor performs on/off control of a conduction state between said second source electrode and said second power line based on said resetting signal; and

wherein said control method further comprises an additional discharging step of turning on said resetting transistor thereby to discharge said holding capacitor and said parasitic capacitor before said pixel data writing step; and

wherein said selection transistor is turned off in said pixel data holding step to float said second gate electrode.

18. The control method according to claim 15, wherein said image display apparatus includes:

a plurality of resetting signal lines to which resetting signals are applied; and

a resetting signal line driver for applying said resetting signals to said resetting signal lines;

wherein each pixel has a resetting transistor having a third drain electrode, a third source electrode, and a third gate electrode, and a parasitic capacitor is formed between said first electrode and said second electrode;

wherein said third drain electrode/said third source electrode is connected to said second source electrode, said third source electrode/ said third drain electrode is connected to said first power line, said third gate electrode is connected to said resetting signal line, and said resetting transistor performs on/off control of a conduction state between said second source electrode and said first power line based on said resetting signal; and

wherein said control method further comprises an additional discharging step of turning on said resetting transistor thereby to discharge said holding capacitor and said parasitic capacitor before said pixel data writing step; and

wherein said selection transistor is turned off in said pixel data holding step to float said second gate electrode.

19. The control method according to claim 15, wherein said pixel display element has a parasitic capacitor between said first electrode and said second electrode; and

wherein said control method further comprises an additional discharging step of turning on said selection transistor and supplying a resetting signal voltage from said signal line thereby to discharge said holding capacitor and said parasitic capacitor before said pixel data writing step; and

wherein said selection transistor is turned off in said pixel data holding step to float said second gate electrode.

20. The control method according to claim 15, wherein said image display apparatus further includes a power supply circuit for supplying a first power voltage and a second power voltage respectively for said first power line and said second power line to said display panel;

wherein said pixel display element has a parasitic capacitor between said first electrode and said second electrode; and

wherein said control method further comprises an additional discharging step of setting said first power voltage to a resetting signal voltage thereby to discharge said holding capacitor and said parasitic capacitor before said pixel data writing step; and

wherein said selection transistor is turned off in said pixel data holding step to float said second gate electrode.

21. The control method according to claim 14, wherein said image display apparatus further includes:

a display panel having a plurality of signal lines to which corresponding gradation pixel data are applied, a plurality of control lines to which control line drive signals are applied, and a plurality of scanning lines to which scanning signals are applied, said pixel being positioned at each of points of intersection between said signal lines and said scanning lines;

a signal line driver for applying said gradation pixel data to said signal lines based on a pixel input signal;

a scanning line driver for applying said scanning signals to said scanning lines; and

a control line driver for applying said control line drive signals to said

control lines;

wherein said pixel has a control transistor having a third drain electrode, a third source electrode, and a third gate electrode;

wherein said selection transistor has a first drain electrode, a first source electrode, and a first gate electrode, said drive transistor has a second drain electrode, a second source electrode, and a second gate electrode, said holding capacitor holds a voltage between said second gate electrode and said second source electrode, and each pixel display element has a first electrode, a second electrode, and a parasitic capacitor between said first electrode and said second electrode;

wherein said first drain electrode/said first source electrode is connected to said signal line, said first source electrode/said first drain electrode is connected to said second gate electrode, said first gate electrode is connected to said scanning line, and said selection transistor performs on/off control of a conduction state between said signal line and said second gate electrode based on said scanning signal;

wherein said first power line is connected to said second source electrode, said drive transistor passes an output current controlled based on a voltage held by said holding capacitor from said second drain electrode to said first electrode;

wherein said third drain electrode/said third source electrode is connected to said second gate electrode, said third source electrode/said third drain electrode is connected to said second drain electrode, said third gate electrode is connected to said control line, and said control transistor performs on/off control of a conduction state between said second gate electrode and

said second drain electrode based on said control line drive signal;

wherein said second power line is connected to said second electrode, and said pixel display element displays a pixel at a gradation based on said output current of said drive transistor; and

wherein said selection transistor is turned on and said control transistor is turned off thereby to write said gradation pixel data from said signal line in said holding capacitor in said pixel data writing step;

said selection transistor is turned off and said control transistor is turned on thereby to discharge charges of said gradation pixel data written in said holding capacitor through said drive transistor for a predetermined time in said discharging step; and

said control transistor is turned off thereby to float said second gate electrode in said pixel data holding step.

22. The control method according to claim 14, wherein said image display apparatus further includes:

a display panel having a plurality of signal lines to which corresponding gradation pixel data are applied, a plurality of control lines to which control line drive signals are applied, and a plurality of scanning lines to which scanning signals are applied, said pixel being positioned at each of points of intersection between said signal lines and said scanning lines;

a signal line driver for applying said gradation pixel data to said signal lines based on a pixel input signal;

a scanning line driver for applying said scanning signals to said scanning lines; and

a control line driver for applying said control line drive signals to said control lines;

wherein said pixel has a control transistor having a third drain electrode, a third source electrode, and a third gate electrode;

wherein said selection transistor has a first drain electrode, a first source electrode, and a first gate electrode, said drive transistor has a second drain electrode, a second source electrode, and a second gate electrode, said holding capacitor holds a voltage between said second gate electrode and said second source electrode, and each pixel display element has a first electrode, a second electrode, and a parasitic capacitor between said first electrode and said second electrode;

wherein said first drain electrode/said first source electrode is connected to said signal line, said first source electrode/said first drain electrode is connected to said second gate electrode, said first gate electrode is connected to said scanning line, and said selection transistor performs on/off control of a conduction state between said signal line and said second gate electrode based on said scanning signal;

wherein said first power line is connected to said second source electrode, said drive transistor passes an output current controlled based on a voltage held by said holding capacitor from said second drain electrode to said first electrode;

wherein said third drain electrode/said third source electrode is connected to said second gate electrode, said third source electrode/said third drain electrode is connected to said second drain electrode, said third gate electrode is connected to said control line, and said control transistor performs

on/off control of a conduction state between said second gate electrode and said first drain electrode based on said control line drive signal;

wherein said second power line is connected to said second electrode, and said pixel display element displays a pixel at a gradation based on said output current of said drive transistor; and

wherein said selection transistor is turned on and said control transistor is turned on thereby to write said gradation pixel data from said signal line in said holding capacitor in said pixel data writing step;

said selection transistor is turned off and said control transistor is turned on thereby to discharge charges of said gradation pixel data written in said holding capacitor through said drive transistor for a predetermined time in said discharging step;

said control transistor is turned off thereby to float said second gate electrode in said pixel data holding step.

23. The control method according to claim 14, wherein said image display apparatus further includes:

a display panel having a plurality of signal lines to which corresponding gradation pixel data are applied, a plurality of control lines to which control line drive signals are applied, and a plurality of scanning lines to which scanning signals are applied, said pixel being positioned at each of points of intersection between said signal lines and said scanning lines;

a signal line driver for applying said gradation pixel data to said signal lines based on a pixel input signal;

a scanning line driver for applying said scanning signals to said scanning

lines; and

a control line driver for applying said control line drive signals to said control lines;

wherein said pixel has a control transistor having a third drain electrode, a third source electrode, and a third gate electrode;

wherein said selection transistor has a first drain electrode, a first source electrode, and a first gate electrode, said drive transistor has a second drain electrode, a second source electrode, and a second gate electrode, said holding capacitor holds a voltage between said second gate electrode and said second source electrode, and each pixel display element has a first electrode, a second electrode, and a parasitic capacitor between said first electrode and said second electrode;

wherein said first drain electrode/said first source electrode is connected to said signal line, said first source electrode/said first drain electrode is connected to said second drain electrode, said first gate electrode is connected to said scanning line, and said selection transistor performs on/off control of a conduction state between said signal line and said second drain electrode based on said scanning signal;

wherein said first power line is connected to said second source electrode, said drive transistor passes an output current controlled based on a voltage held by said holding capacitor from said second drain electrode to said first electrode;

wherein said third drain electrode/said third source electrode is connected to said second gate electrode, said third source electrode/said third drain electrode is connected to said second drain electrode, said third gate

electrode is connected to said control line, and said control transistor performs on/off control of a conduction state between said second gate electrode and said second drain electrode based on said control line drive signal;

wherein said second power line is connected to said second electrode, and said pixel display element displays a pixel at a gradation based on said output current of said drive transistor; and

wherein said selection transistor is turned on and said control transistor is turned on thereby to write said gradation pixel data from said signal line in said holding capacitor in said pixel data writing step;

said selection transistor is turned off and said control transistor is turned on thereby to discharge charges of said gradation pixel data written in said holding capacitor through said drive transistor for a predetermined time in said discharging step; and

said control transistor is turned off thereby to float said second gate electrode in said pixel data holding step.

24. The control method according to claim 14, wherein said image display apparatus further includes:

a display panel having a plurality of signal lines to which corresponding gradation pixel data are applied, a plurality of control lines to which control line drive signals are applied, and a plurality of scanning lines to which scanning signals are applied, said pixel being positioned at each of points of intersection between said signal lines and said scanning lines;

a signal line driver for applying said gradation pixel data to said signal lines based on a pixel input signal;

a scanning line driver for applying said scanning signals to said scanning lines; and

a control line driver for applying said control line drive signals to said control lines;

wherein said pixel has a control transistor having a third drain electrode, a third source electrode, and a third gate electrode, and an input drive transistor having a fourth drain electrode, a fourth source electrode, and a fourth gate electrode;

wherein said selection transistor has a first drain electrode, a first source electrode, and a first gate electrode, said drive transistor has a second drain electrode, a second source electrode, and a second gate electrode, said holding capacitor holds a voltage between said second gate electrode and said second source electrode, and each pixel display element has a first electrode, a second electrode, and a parasitic capacitor between said first electrode and said second electrode;

wherein said first drain electrode/said first source electrode is connected to said signal line, said first source electrode/said first drain electrode is connected to said third drain electrode/said third source electrode, said first gate electrode is connected to said scanning line, and said selection transistor performs on/off control of a conduction state between said signal line and said third drain electrode/said third source electrode based on said scanning signal;

wherein said first power line is connected to said second source electrode, said drive transistor passes a first output current controlled based on a voltage held by said holding capacitor from said second drain electrode to said first electrode;

wherein said third drain electrode/said third source electrode is connected to said first source electrode/said first drain electrode, said third source electrode/said third drain electrode is connected to said second gate electrode, said third gate electrode is connected to said control line, and said control transistor performs on/off control of a conduction state between said first source electrode/said first drain electrode and said second gate electrode based on said control line drive signal;

wherein said first power line is connected to said fourth source electrode, said fourth drain electrode is connected to said first source electrode/said first drain electrode, said fourth gate electrode is connected to said second gate electrode, said input drive transistor passes a second output current controlled based on a voltage between said fourth source electrode and said fourth gate electrode from said fourth source electrode to said fourth drain electrode;

wherein said second power line is connected to said second electrode, and said pixel display element displays a pixel at a gradation based on said first output current of said drive transistor; and

wherein said selection transistor is turned on and said control transistor is turned on thereby to write said gradation pixel data from said signal line in said holding capacitor in said pixel data writing step;

said selection transistor is turned off and said control transistor is turned on thereby to discharge charges of said gradation pixel data written in said holding capacitor through said input drive transistor for a predetermined time in said discharging step; and

said control transistor is turned off thereby to float said second gate electrode in said pixel data holding step.

25. The control method according to claim 13, wherein said image display apparatus further includes:

a display panel having a plurality of signal lines to which corresponding gradation pixel data are applied, a plurality of control lines to which control line drive signals are applied, and a plurality of scanning lines to which scanning signals are applied, said pixel being positioned at each of points of intersection between said signal lines and said scanning lines;

a signal line driver for applying said gradation pixel data to said signal lines based on a pixel input signal;

a scanning line driver for applying said scanning signals to said scanning lines; and

a control line driver for applying said control line drive signals to said control lines;

wherein said pixel has a control transistor having a third drain electrode, a third source electrode, and a third gate electrode, and an input drive transistor having a fourth drain electrode, a fourth source electrode, and a fourth gate electrode;

wherein said selection transistor has a first drain electrode, a first source electrode, and a first gate electrode, said drive transistor has a second drain electrode, a second source electrode, and a second gate electrode, said holding capacitor holds a voltage between said second gate electrode and said second source electrode, and each pixel display element has a first electrode, a second electrode, and a parasitic capacitor between said first electrode and said second electrode;

wherein said first drain electrode/said first source electrode is connected

to said signal line, said first source electrode/said first drain electrode is connected to said third drain electrode/said third source electrode, said first gate electrode is connected to said scanning line, and said selection transistor performs on/off control of a conduction state between said signal line and said third drain electrode/said third source electrode based on said scanning signal;

wherein said first power line is connected to said second source electrode, said drive transistor passes a first output current controlled based on a voltage held by said holding capacitor from said second drain electrode to said first electrode;

wherein said third drain electrode/said third source electrode is connected to said first source electrode/said first drain electrode and said fourth gate electrode, said third source electrode/said third drain electrode is connected to said second gate electrode, said third gate electrode is connected to said control line, and said control transistor performs on/off control of a conduction state between said first source electrode/said first drain electrode and said second gate electrode based on said control line drive signal;

wherein said first power line is connected to said fourth source electrode, said fourth drain electrode is connected to said first source electrode/said first drain electrode, said fourth gate electrode is connected to said fourth drain electrode, said input drive transistor passes a second output current controlled based on a voltage between said fourth source electrode and said fourth gate electrode from said fourth source electrode to said fourth drain electrode;

wherein said second power line is connected to said second electrode, and said pixel display element displays a pixel at a gradation based on said first output current of said drive transistor; and

wherein said selection transistor is turned on and said control transistor is turned on thereby to write said gradation pixel data from said signal line in said holding capacitor in said pixel data writing step;

said selection transistor is turned off and said control transistor is turned on thereby to discharge charges of said gradation pixel data written in said holding capacitor through said input drive transistor for a predetermined time in said discharging step; and

said control transistor is turned off thereby to float said second gate electrode in said pixel data holding step.

26. The control method according to claim 14, wherein said pixel display element comprises an organic electroluminescence element.

27. A drive circuit for a current control element, comprising:

a drive transistor and a pixel display element which are connected in series between a first power line and a second power line;

a holding capacitor connected to a gate electrode of said drive transistor; and

a selection transistor connected between a signal line and the gate electrode of said drive transistor;

wherein said selection transistor is turned on to input a first signal voltage from said signal line to discharge signal charges written in said holding capacitor through said drive transistor in a selection period of said drive circuit, thereafter a second signal voltage is input from said signal line and held in said holding capacitor, and said selection transistor is turned off to pass a current

through said drive transistor to said current control element in a non-selection period of said drive circuit.

28. The drive circuit according to claim 27, wherein said holding capacitor is connected between a junction between said drive transistor and said current control element and the gate electrode of said drive transistor.

29. The drive circuit according to claim 27, wherein a resetting signal voltage is input to said signal line to reset charges stored in said holding capacitor and a parasitic capacitor of said current control element in an initial stage of the selection period of said drive circuit.

30. The drive circuit according to claim 27, wherein said drive transistor is turned on to set said first power line to a resetting signal voltage thereby to reset charges stored in said holding capacitor and a parasitic capacitor of said current control element in an initial stage of the selection period of said drive circuit.

31. The drive circuit according to claim 27, wherein each of said selection transistor and said drive transistor comprises an N-channel field-effect transistor.

32. The drive circuit according to claim 27, wherein each of said selection transistor and said drive transistor comprises a P-channel field-effect transistor.

33. The drive circuit according to claim 27, further comprising:

a switching transistor between the gate and source electrodes of said drive transistor;

wherein said switching transistor is turned on to reset charges stored in said holding capacitor and a parasitic capacitor of said current control element in an initial stage of the selection period or the non-selection period of said drive circuit.

34. The drive circuit according to claim 27, further comprising:

a switching transistor between the gate electrode of said drive transistor and said second power line;

wherein said switching transistor is turned on to reset charges stored in said holding capacitor and a parasitic capacitor of said current control element in an initial stage of the selection period or the non-selection period of said drive circuit.

35. The drive circuit according to claim 33, wherein each of said selection transistor, said drive transistor, and said switching transistor comprises an N-channel field-effect transistor.

36. The drive circuit according to claim 34, wherein each of said selection transistor, said drive transistor, and said switching transistor comprises an N-channel field-effect transistor.

37. The drive circuit according to claim 33, wherein each of said

selection transistor, said drive transistor, and said switching transistor comprises a P-channel field-effect transistor.

38. The drive circuit according to claim 34, wherein each of said selection transistor, said drive transistor, and said switching transistor comprises a P-channel field-effect transistor.

39. A drive method for a drive circuit including a drive transistor and a pixel display element which are connected in series between a first power line and a second power line, a holding capacitor connected to a gate electrode of said drive transistor, and a selection transistor connected between a signal line and the gate electrode of said drive transistor, the drive method comprising the steps of:

turning on said selection transistor to input a first signal voltage from said signal line to discharge signal charges written in said holding capacitor through said drive transistor in a selection period of said drive circuit;

inputting a second signal voltage from said signal line and holding the second signal voltage in said holding capacitor; and

turning off said selection transistor to pass a current through said drive transistor to said current control element in a non-selection period of said drive circuit.

40. The drive method according to claim 39, wherein said holding capacitor is connected between a junction between said drive transistor and said current control element and the gate electrode of said drive transistor.

41. The drive method according to claim 39, wherein a resetting signal voltage is input to said signal line to reset charges stored in said holding capacitor and a parasitic capacitor of said current control element in an initial stage of the selection period of said drive circuit.

42. The drive method according to claim 39, wherein said drive transistor is turned on to set said first power line to a resetting signal voltage thereby to reset charges stored in said holding capacitor and a parasitic capacitor of said current control element in an initial stage of the selection period of said drive circuit.

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☑ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.